Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **1 N. PRE**
2. **1Q**
3. **1 N.Q**
4. **GND**
5. **2 N. Q**
6. **2Q**
7. **2 N. PRE**
8. **2 CLK**
9. **2D**
10. **2 N. CLR**
11. **VCC**
12. **1 N. CLR**
13. **1D**
14. **1 CLK**

**.054”**

**8 7**

**9**

**10**

**11**

**12**

**13**

**6**

**5**

**4**

**3**

**2**

**.056”**

**MASK**

**REF**

**ACT11074**

**14 1**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: ACT11074**

**APPROVED BY: DK DIE SIZE .054” X .056” DATE: 5/23/17**

**MFG: TIH THICKNESS .019” P/N: 54ACT74**

**DG 10.1.2**

#### Rev B, 7/1